AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. – 2. (Cancelled)

3. (Previously Presented) The method of claim 6, the step of asserting a lock signal further comprising the step of:

asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains two memory address data.

4. – 5. (Cancelled)

6. (Previously Presented) A method of controlling access to a shared memory of a multiprocessor system, the multiprocessor system comprising a first bus and a second bus coupled to the shared memory, the first bus coupled to a first processor, and the second bus coupled to a second processor, the method comprising the steps of:

requesting exclusive access to a first memory location of the shared memory by the first processor;

granting exclusive access to the first memory location of the shared memory to the first processor;

allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location; and

storing access request information associated with the exclusive access in a first register in a first memory controller and in a second register in a second memory controller,

the step of requesting exclusive access comprising the steps of:

asserting a lock signal on the first bus;

sending a lock request from the first processor to the first memory controller coupled to the first bus, the second bus, and the shared memory;

forwarding the lock request from the first memory controller to a switch; and

signaling the first processor to retry the lock request,

the step of granting exclusive access comprising the steps of:

signaling the first memory controller by the switch to retry the lock request;

assigning exclusive access to the first memory location by the switch;

notifying the first memory controller of the exclusive access assigned in the assigning step; and

granting exclusive access to the first memory location by the first memory controller responsive to a retry of the lock request by the first processor,

the step of assigning exclusive access to the first memory location by the switch comprising the steps of:

determining if the first memory location is currently assigned;

saving the access request information in a register in the switch if the first memory location is not currently assigned;

sending the access request information to the first memory controller; and

sending the access request information to the second memory controller.

7. (Previously Presented) The method of claim 6, the access request information comprising:

a node ID of the first processor;

a cycle ID of the first processor; and

memory address data for the first memory location.

8. (Original) The method of claim 7, the memory address data comprising:

a first memory address; and

a second memory address,

wherein the first memory address can be non-contiguous with the second memory address.

9. (Previously Presented) The method of claim 6, further comprising the step of:

releasing exclusive access to the first memory location.

10. (Previously Presented) A method of controlling access to memory of a multinodal computer system, the multinodal computer system comprising a plurality of multiprocessor nodes, the method comprising the steps of:

requesting exclusive access to a first memory location of a shared memory in a first multiprocessor node of the plurality of multiprocessor nodes by a first processor of the first multiprocessor node;

granting exclusive access to the first memory location of the shared memory to the first processor;

allowing access to a second memory location of the shared memory to a second processor of a second multiprocessor node of the plurality of multiprocessor nodes while the first processor has exclusive access to the first memory location;

communicating between the multiprocessor nodes through a switch; and

sending, by the switch, access request information associated with the exclusive access of the shared memory of the first multiprocessor node to the second multiprocessor node.

11. (Previously Presented) The method of claim 10, the requesting step comprising:

asserting a lock signal on a first bus, the first bus coupling the first processor and a first memory controller of the first multiprocessor node; and

sending a lock request to the first memory controller;

forwarding the lock request from the first memory controller to the switch, the switch coupled to each of the plurality of multiprocessor nodes.

12. (Previously Presented) The method of claim 11, the shared memory comprising:

a first memory coupled to the first memory controller; and

a second memory coupled to a second memory controller in the second multiprocessor node of the plurality of multiprocessor nodes.

13. (Original) The method of claim 12, the step of asserting a lock signal comprising the step of:

asserting a split lock signal on the first bus, the split lock signal indicating that the lock request contains a first memory address data and a second memory address data.

14. (Original) The method of claim 13, the first memory address data referencing the first memory and the second memory address data referencing the second memory.

15. (Original) The method of claim 13, the first memory address data referencing the second memory and the second memory address data referencing the first memory.

16. (Previously Presented) The method of claim 11, the step of requesting exclusive access further comprising:

signaling the first processor to retry the lock request.

17. (Previously Presented) The method of claim 11, the step of granting exclusive access comprising the steps of:

signaling the first memory controller to retry the lock request;

assigning exclusive access to the first memory location by the switch;

notifying the first memory controller of the exclusive access assigned in the assigning step; and

assigning exclusive access to the first memory location by the first memory controller responsive to a retry of the lock request by the first processor.

18. (Previously Presented) The method of claim 17, the step of assigning exclusive access to the first memory location by the switch comprising the steps of:

determining if the first memory location is currently assigned;

saving the access request information associated with the exclusive access if the first memory location is not current assigned; and

broadcasting the access request information to each memory controller of each of the plurality of multiprocessor nodes.

19. (Previously Presented) The method of claim 18, the access request information comprising:

a node ID of the first multiprocessor node;

a cycle ID of the first processor; and

a memory address data for the first memory location.

20. (Original) The method of claim 10, further comprising the step of:

releasing exclusive access to the first memory location.

21. (Cancelled)

22. (Previously Presented) A computer system for utilizing a shared memory, the computer system comprising:

a first multiprocessor node, comprising:

a first processor bus;

a first processor, coupled to the first processor bus, the first processor comprising:

circuitry to generate an exclusive access request for a first memory location,

a second processor bus;

a second processor, coupled to the second processor bus, the second processor adapted to:

request access to a second memory location;

a first memory;

a first memory controller, coupled to the first processor bus, the second processor bus, and the first memory, the first memory controller adapted to:

allow exclusive access to the first memory location by the first processor; and

allow access to the second memory location by the second processor while the first processor has exclusive access to the first memory location;

a second multiprocessor node, comprising:

a third processor bus;

a third processor, coupled to the third processor bus, the third processor adapted to:

request access to a third memory location;

a second memory;

a second memory controller, coupled to the third processor bus, and the first memory, the second memory controller adapted to:

allow exclusive access to the first memory location by the first processor;

allow access to the second memory location by the second processor while the first processor has exclusive access to the first memory location; and

allow access to the third memory location by the third processor while the first processor has exclusive access to the first memory location; and

a switch, coupled to the first memory controller and the second memory controller, for switching transactions between the first multiprocessor node and the second multiprocessor node.

23. (Original) The computer system of claim 22, the first memory location comprising:
a first portion in the first memory; and
a second portion in the second memory.

24. (Original) The computer system of claim 22,
wherein the first memory location is in the first memory, and
wherein the second memory location is in the first memory.

25. (Original) The computer system of claim 22,
wherein the first memory location is in the first memory, and
wherein the third memory location is in the first memory.

26. (Original) The computer system of claim 22,
wherein the first memory location is in the second memory, and
wherein the third memory location is in the second memory.

27. (Original) The computer system of claim 22,
wherein the first memory location is in the second memory, and
wherein the third memory location is in the first memory.

28. (Original) The computer system of claim 22, the switch comprising:
a lock register for storing a lock control information.

29. (Original) The computer system of claim 28, the lock control information comprising:
a node ID corresponding to the first processor;
a cycle ID corresponding to the first processor; and
a first memory address corresponding to the first memory location.

30. (Original) The computer system of claim 29, the lock control information further comprising:
a second memory address corresponding to the first memory location.

31. (Previously Presented) The computer system of claim 29, the switch comprising:
circuitry to signal the first memory controller to retry allowing exclusive access to the first memory location by the first processor;
circuitry to arbitrate among requests for exclusive access to the first memory location;
circuitry to broadcast the lock control information to the first memory controller and the second memory controller.

32. (Original) The computer system of claim 31, the first memory controller further comprising:
circuitry to signal the first processor to retry the exclusive access request;
circuitry to shadow the lock control information broadcast by the switch; and
the second memory controller further comprising:
circuitry to shadow the lock control information broadcast by the switch.

33. (Original) The computer system of claim 30, wherein the first memory address can be in either the first memory or the second memory, and

wherein the second memory address can be in either the first memory or the second memory.

34. (Previously Presented) A method of controlling access to a shared memory of a multiprocessor system, the multiprocessor system comprising a first bus and a second bus coupled to the shared memory, the first bus coupled to a first processor, and the second bus coupled to a second processor, the method comprising the steps of:

requesting exclusive access to a first memory location of the shared memory by the first processor;

granting exclusive access to the first memory location of the shared memory to the first processor;

allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location;

wherein requesting exclusive access comprises:

sending a lock request from the first processor to a first memory controller coupled to the shared memory;

forwarding the lock request from the memory controller to a switch; and

the switch broadcasting lock request information to the first memory controller and at least another memory controller.

35. (Previously Presented) The method of claim 34, further comprising:

each of the first memory controller and at least another memory controller storing the lock request information.

36. (Previously Presented) The method of claim 35, further comprising the switch storing the lock request information in a register in the switch,

wherein the memory controllers also store the lock request information in respective registers in the memory controllers.

37. (Previously Presented) The method of claim 6, wherein the access request information in the second register in the second memory controller is a shadow copy of the access request information in the first register in the first memory controller.

38. (Previously Presented) The method of claim 10, further comprising:

the switch forwarding the access request information to a second memory controller in the second multiprocessor node; and

the second memory controller storing the access request information in the second memory controller.

39. (Previously Presented) The method of claim 10, further comprising:

storing the access request information in a first register of a first memory controller in the first multiprocessor node and in a second register in a second memory controller in the second multiprocessor node.

40. (Previously Presented) The method of claim 39, further comprising storing the access request information in a register in the switch,

wherein the access information in the first register of the first memory controller and in the second register of the second memory controller are shadow copies of the access request information in the register of the switch.

41. (Previously Presented) A multiprocessor system comprising:

a plurality of multiprocessor nodes, each of the multiprocessor nodes comprising:

a shared memory;

a processor to request exclusive access of a memory location in the shared memory;

a memory controller to forward access request information associated with the exclusive access from the multiprocessor node for storage of the access request information in another multiprocessor node, the memory controller including a register; and

a switch coupled to the multiprocessor nodes, the switch to receive the access request information and to send the access request information to the multiprocessor nodes for storage of the access request information in the respective registers of the memory controllers.

42. (Currently Amended) The multiprocessor system of claim [[42]] 41, wherein the switch includes a register to store the access request information,

wherein the access request information in the registers of the respective memory controllers are shadow copies of the access request information in the register of the switch.